4.3.3 On/Off Control and Low Battery Shutdown

Quad CMOS gate U5 is powered at all times from Vp, with its supply voltage limited to a safe value by Zener diode CR7. This zener voltage was selected so that it draws no current when only battery power is available. This prevents discharging the battery when the unit is off. The bistable flip-flop U5A and U5B stores the on/off state of the monitor and is set and reset by the front panel ON and OFF switches. The output of this flip-flop drives the base of the emitter-follower, Q12, whose output is one junction drop below the CMOS gate supply voltage. Thus, this switched supply is limited to about 13.4 Vdc. This emitter-follower output supplies power to reference shunt regulator, U4, and the emitter of Q8. When the emitter of Q12 is at least one junction drop above the reference voltage, Q8 conducts and supplies power (Vs) to the comparator U1A, turning on the regulated supplies. Vs is fed back to latch the bistable flip-flop. If the input voltage falls below the threshold set by U4, Vs turns off, removing power from the comparator. This action turns off the monitor and unlatches the on/off flip-flop, preventing the monitor from deep discharging the battery. R34 supplies a small amount of positive feedback to reference U4 for threshold hysteresis and fast switching of Vs.

4.3.4 Logic System Master Reset Circuit

When Vs is off, gate U5 turns on FET Q10, holding the reset line (RESET-0) asserted. When Vs switches on, C13 begins to charge through R42. After a delay of about 40 to 104 milliseconds, RESET-0 is unasserted and allows the processor to start. Diode, CR15, discharges C13 through R33 and the open-collector output of U5-3 quickly upon removal of Vs to re-arm the time delay circuit.

4.3.5 Battery Charger Circuit

When line power is available, the switching regulator U3 receives power from a separate DC supply, Vbc, supplied by rectifiers CR8 and CR9. This IC drives switching transistor Q11 which supplies power from Vp to charge the battery. Resistor R30 senses the charging current and turns on Q6 when the current exceeds about 350 milliamps. Q6 drives the current limit input of U3, reducing the pulse width. FET Q2 disconnects the feedback network from the battery when the battery charger is not operating so the battery is not discharged. R12 adjusts the maximum output voltage (float) to the proper value for the battery (generally 13.65 Vdc).

4.4 CPU BOARD OPERATION

The CPU board circuits are shown on schematic SC315-293 contained in Section 6. The circuits are divided into 7 functional circuits;

- the microprocessor system,
- the analog subsystem,
- the switchpanel interface circuits,
- the display board interface circuits,
- the pneumatics module interface circuits,
- the fail-safe timer circuit, and
- the external communications & control circuits.

4.4.1 Microprocessor System

The microprocessor system consists of a master clock circuit, a CMOS 8-bit microprocessor, a custom-designed gate array circuit, a 32K x 8 EPROM circuit, one 8K x 8 Static RAM, an analog-to-digital converter with digital I/O, and a digital output latch.

4.4.1.1 MASTER CLOCK CIRCUIT. The master clock circuit is shown on sheet 2 of the schematic. It consists of CMOS inverter, U9, R1, R2, C1, C2, C3 and Y1, configured to form a crystal-controlled oscillator. The clock circuit oscillates between CMOS logic levels at a fundamental frequency of 3.6864 MHz. The master clock is sent directly to the gate array, U2, where it is divided down to provide the E and Q clocks for the CPU at 0.9216 Mhz, the 2 millisecond FIRQ interrupt, and the 1.8432 MHz clock (UCLK) for the Asynchronous Communications Interface Adapter (ACIA) .

4.4.1.2 MICROPROCESSOR CIRCUIT. The microprocessor circuit is shown on sheet 2 of the schematic. The microprocessor, U1, is a CMOS 6309E, 8-bit processor. It has an 8-bit bidirectional data bus and a 16-bit address bus which it uses to address the stored program in the 32K EPROM and to communicate with various I/O devices. Temporary storage (as long as power is on) for data generated by the operating program is provided by two, 8K by 8-bit CMOS static RAM's.

The 6309E requires externally generated E (U1-34) and Q (U1-35) clock pulses and these are derived from the master clock and generated by the gate array, U2. The interrupt request line at U1-3, IRQ, is driven by the ACIA interrupt which is enabled or disabled under software control. The interrupt request line at U1-4, FIRQ, is driven by the 1200 Hz interrupt generated by the gate array, U2, which triggers all the background tasks performed by the operating program. The read/write line at U1-32 is controlled by the microprocessor and is used by the gate array (U2), the ACIA (U6), and the a/d converter and digital I/O (U7), for gating data transfers from or to the data bus.

The reset line (U1-37) is driven by the power supply module through connector J5-18 in response to POWER ON and POWER OFF switch depressions.

4.4.1.3 GATE ARRAY CIRCUIT. The gate array circuit is shown on sheet 2 of the schematic. It is a custom -designed circuit that provides for high order address decoding, dividing the master clock to obtain various clock functions, controlling the processor interrupt (FIRQ), controlling the failsafe timer reset pulse, and discrete digital I/O.

High order address decoding is provided for addressing certain internal functions, for generating certain select signals for devices external to the gate array, and for generating certain discrete digital I/O signals. The following table defines the addresses decoded, specifies their function and, where applicable, shows the output pin and signal name:

4.4.1
Microprocessor System
Continued

ADDRESS	FUNCTION	PIN #	SIGNAL
0000H to 07FFH	OUTPUT LATCH (U8) SELECT	U2-10	LTCHSEL-0
0800H to 0FFFH	FRONT PANEL DISPLAY SELECT	U2-39	DSPLSEL-0
1000H to 1FFFH	Not Used	-	-
2000H to 27FFH	A-to-D CONVERTER (U7) SELECT	U2-36	A/DSEL-0
2800H to 2FFFH	SERIAL INTERFACE (U6) SELECT	U2-17	ACIASEL-0
3000H to 30FFH	AUDIO ANNUNCIATOR	U2-33	BEEPER-1
3100H to 31FFH	Not Used	-	-
3200H to 32FFH	PNEUMATIC PUMP CONTROL	U2-31	PUMPON-1
3300H to 33FFH	DEFLATE VALVE CONTROL	U2-28	DEFLATE-0
3400H to 34FFH	EXT. COMMUNICATION CONTROL	U2-27	RXRRESET-0
3500H to 35FFH	EXT. COMMUNICATION CONTROL	U2-30	TXENAB-1
3600H to 36FFH	EXT. EQUIPMENT CONTROL	U2-25	AUXOUT-0
3700H to 37FFH	Not Used	-	-
3800H to 38FFH	SET FAIL-SAFE TIMER	U2-34	ZDMANB-0
3900H to 39FFH	ENABLE/DISABLE 1200 Hz INT.	Internal	-
3A00H to 3AFFH	CLEAR 1200 Hz FLAG/DEACT. INT.	Internal	-
3B00H to 3BFFH	READ 1200 Hz FLAG	U2-23	D7
3C00H to 3CFFH	RE-ARM FAIL-SAFE LOGIC	Internal	-
3D00H to 3DFFH	Not Used	-	-
3E00H to 3EFFH	READ AUX. INPUT	U2-40	AUXIN-0
3F00H to 3FFFH	COMPARE FAIL-SAFE TIMER	U2-35	U11-9
4000H to 7FFFH	RAM (U5) SELECT	U2-8	ZMCS1B-0
8000H to BFFFH	Spare Socket	U2-9	ZMCS2B-0
C000H to FFFFH	Not Decoded (ROM program)	-	-

A clock divider circuit which accepts the master clock pulse at U2-2 (ZOSC) and divides it down to 921.6 kHz to produce the quadrature E and Q clock pulses at U2-7 and U2-5, respectively. These quadrature clocks are also exclusive ORred within the gate array to produce the 1.8432 MHz clock signal (ZUCLK) which is output at U2-29 and sent to the ACIA circuit (U6) to control the Baud rate. Also, the Q clock (921.6 kHz) is divided within the gate array by 768 to produce a 1200 Hz signal used by the gate array interrupt control logic.

The interrupt control logic is under software control and allows the CPU to read or clear the state of an internal 1200 Hz timer flag and enable or disable the 1200 Hz interrupt (ZTIRQB). The internal 1200 Hz signal is used to set a flag in the gate array which may be read by the CPU by executing a read instruction of location 3B00H. A read to this location causes the gate array to gate the state of the 1200 Hz flag to the output (ZD7D) at U2-23 which is connected to bit 7 (D7) of the data bus. The 1200 Hz flag can be cleared by the CPU by writing anything to address 3A00H (this will also clear the interrupt if it was enabled). The 1200 Hz interrupt (ZTIRQB) may be enabled by writing a ONE in data bit 7 to address 3900H or disabled by writing a ZERO in data bit 7 to address 3900H)all other data bits are ignored). The interrupt (ZTIRQB) is output to the CPU at U2-4 whenever it is enabled and the 1200 Hz flag is set.

4.4.1
Microprocessor System
Continued

The fail-safe timer reset pulse (U2-34) is driven by control logic in the gate array that responds only to the proper sequence of certain software commands. In this way, the logic provides a system check of the microprocessor software execution in the process of generating the fail-safe timer reset pulse. The proper software sequence is:

1. Write 80H or higher to address 3800H.
2. Write 7FH or lower to address 3C00H.

The first instruction causes the gate array logic to generate a fail-safe timer reset pulse (ZDMANB) at U2-34. The signal goes low for one E clock cycle and then returns high. The second instruction re-arms the gate array software monitoring logic to detect the following error conditions:

1. Any write of 7FH or below to any address between 3800H and 38FFH, inclusive.
2. Any read of address 3800H to 38FFH, inclusive.
3. Two consecutive writes of 80H or above to any address between 3800H and 38FFH, inclusive, without an intervening write of 7FH or below to any address between 3800H and 38FFH, inclusive.
4. Any write of 80H or above to any address between 3C00H and 3CFFH, inclusive.
5. Any read of address 3C00H to 3CFFH, inclusive.
6. Two consecutive writes of 7FH or below to any address between 3C00H and 3CFFH, inclusive, without an intervening write of 80H or above to any address between 3800H and 38FFH, inclusive.

If any of these error conditions occur, the gate array logic sets a latch that disables the fail-safe timer reset strobe from being output to U2-34 and, thus, allow the fail-safe timer to time out in 4 seconds and produce the fail-safe alarm.

Discrete digital inputs are read from bit 7 (D7) on the data bus when reading the appropriate address. Discrete digital outputs are generated by writing to the appropriate address with the desired data on bit 7 (D7) of the data bus. The appropriate addresses, signal name, and logic state are shown in the address map above.

4.4.1
Microprocessor System
Continued

4.4.1.4 EPROM CIRCUIT. The operating program for the monitor is stored in U4, a CMOS 32K x 8 EPROM. The memory responds to addresses C000H through FFFFH with bit 15 of the address bus (A15) enabling the EPROM at U4-20 through inverter U9-10.

4.4.1.5 RAM CIRCUIT. One CMOS 8K x 8 static RAM is provided in location U5. This provides temporary storage for a CPU scratchpad and for storing prior determination data. It is also used for storage of diagnostic programs which may be down-loaded through the communications port and executed by the CPU. The RAM is selected by the high-order address decode, ZMCS1B, which is produced by the gate array, U2, allowing the RAM to respond to addresses in the range of 4000H to 7FFFH.

4.4.1.6 A/D CONVERTER WITH DIGITAL I/O. The analog-to-digital converter (U7, shown on sheet 3) is a CMOS, 16 channel, 8-bit A-to-D which also provides some digital I/O. The circuit is powered by the +5 Vdc logic supply at U7-39 and provided with the voltage reference (Vref) at U7-40. I/O transfers and a-to-d conversions are controlled by the chip select A/DSEL-0 (asserted by the gate array for addresses 2000H through 27FFH) at U7-20, the read/write line at U7-17, the CPU E clock at U7-18, and address bit A1 at U7-19. Address bit A1 is used internally by the converter to select control and data registers and to control double-byte transfers.

Dedicated digital inputs DI3 through DI5 are used to read the state of jumpers JMP21 through JMP19, respectively. JMP 21 has no use in the normal operation of the monitor and should not be inserted. JMP 20 controls the CUFF pressure display in the MAP window. When no jumper is installed in JMP 20, the CUFF pressure at each deflation step is alternately displayed with the previous MAP determination. When JMP 20 is installed, only CUFF pressure is displayed in the MAP window during a stepped deflation. JMP 19 controls whether pressure is displayed as mmHg or kPa. When no jumper is installed in JMP 19, the pressure displays show pressure in mmHg. When JMP 19 is installed, the pressure displays show pressure in kPa.

DIO0 through DIO2 are programmable digital I/O lines. The operating program in the monitor programs these to be digital outputs at power on time and sequentially strobes these outputs as a background task to scan the switch panel matrix as KEYROW0, KEYROW1 and KEYROW2. CR13, CR14 and CR15 are used to preclude the possibility of simultaneous keyswitch closures burning out a digital output stage.

4.4.1
Microprocessor System
Continued

Shared digital ports (P0 - P5) interpret the voltage present on these pins (U7-27 thru U7-22) as digital inputs. P0 through P3 are assigned to KEYCOL0 through KEYCOL3, respectively , and are used to sense keyswitch closures when KEYROW0 thru KEYROW2 are output. P4 (U7-23) samples the square wave output of the temperature detection circuit voltage-to-frequency converter applied to JMP 22. P5 (U7-22) sense the occurrence of an overpressure condition, OP-1, which is sent from the pneumatics module via J3-12.

The nine analog input channels, AN0 through AN9 (there is no AN1), allow for digitizing (0 - 255) analog voltages in the range of +0 Vdc to +5 Vdc. The channel assignments are as follows:

CHAN	SIG	SOURCE
AN0	PT	This is the cuff pressure transducer signal in the range of +0 to +4.5 Vdc.
AN2	FPT	This is the filtered (AC coupled) pressure transducer signal (pulsatile complexes) in the range of +0 to +4.5 Vdc.
AN3	+5V	This is the +5 Vdc logic supply from the power supply at J5-5,6.
AN4	+8V	This is the +8 Vdc supply from the power supply at J5-9,10.
AN5	-V	This is the -6.2 Vdc nominal analog supply applied to Vref across R64 and R65 to give a positive representative voltage.
AN6	Vbs	This is the battery voltage divided by 3 from the power supply at J5-13.
AN7	Vbc	This is the battery charging voltage applied across voltage divider R66 and R67 representative of 13.6 to 30 Vdc.
AN8	PTEX V	This is the pressure transducer excitation voltage applied to pin 1 of the pressure transducer (TX1).
AN9	VLVSENSE	This is the voltage across R86 which is representative of the current drain of the valve coils in the pneumatics module brought in at J3-40. This is used only during manufacturing testing .

4.4.1 Microprocessor System Continued

4.4.1.7 DIGITAL OUTPUT LATCH CIRCUIT. The digital output latch (U8) is shown on sheet 3 of the schematic. This circuit contains 8 CMOS flip-flops which have a common clock input at U8-11. The D inputs are steered by the microprocessor data bus and clocked by NAND gate, U10. U10 is enabled by LTCHSEL-0 which is generated by the gate array in response to an address in the range of 0000H to 07FFH. The output of U10 goes low during the Q clock and then, on the trailing edge of the Q clock, goes high to latch the data. The outputs of the latch control the offsets of the pressure transducer amplifier circuits, the filtered pressure transducer circuit test pulse (FPTTEST-1), and the zero and dump valve control signals (ZERO-1 and DUMP-0) which are sent to the pneumatics module via J3-16 and J3-15, respectively.

4.4.2 Analog Subsystem

The following circuits comprise the analog subsystem:

- Negative bias supply circuit
- Pressure transducer and preamp circuit
- Automatic zero setting circuit
- Oscillation channel amplifier circuit
- Reference voltage supply circuit
- Power supply voltage monitors

4.4.2.1 NEGATIVE BIAS SUPPLY CIRCUIT. A negative bias voltage supply is generated from the +8 volt supply on the CPU board to provide the negative rail for the analog circuitry. This negative supply circuit is shown on sheet 1 of the schematic. Three sections of U18 comprise an oscillator operating at about 20 kHz. Two sections of U18 buffer the output of this oscillator and drive the output amplifier made up of transistors Q3 and Q4, the output of which is a rectangular waveform of about 7.4 volts p-p. C24 and CR9 serve as a clamping level shifter to translate the pulse waveform such that the voltage at CR9 switches between +0.7 Vdc and -6.7 Vdc. CR8 rectifies this negative pulse to provide a supply of about -6.0 volts across C25, which filters out the switching components.

4.4.2
Analog Subsystem
Continued

4.4.2.2 PRESSURE TRANSDUCER CIRCUIT. Pressure transducer TX1 is excited by a constant current generator comprising Q1, Q2, and a section of U20. The current through the transducer is controlled by R17, which limits the current to 13.5 milliamperes. R16 provides the correct source impedance for proper temperature compensation of the pressure transducer. The output of the transducer, 40 to 60 mV at 255 mmHg pressure, is amplified by the differential amplifier using two additional sections of U20. The zero pressure offset of TX1 as well as the offset of the preamp are coarsely nulled by a voltage set by R33 (PT ZERO) and buffered by the fourth section of U20. The scale factor is calibrated by R20 (SCALE ADJUST) trimmer and the gain of a section of U14 to be 1.00 mmHg/ADU, providing a nominal gain of 100 from the transducer to the A/D converter. CR3, CR4, and two sections of U14 serve to constrain the output of the transducer amplifier to voltages between 0 and 5.0 volts to ensure proper operation of the A/D converter.

4.4.2.3 AUTOMATIC ZERO SETTING CIRCUIT. Auto Zero of the transducer channel is accomplished mainly in software. During calibration the coarse offset trimmer is set for an A/D reading of 17. During auto zero, the processor activates the zero valve, records the PT reading, and subtracts this reading from subsequent pressure readings. In order to preserve the capability of reading pressures above 200 mmHg, the signal "DASH50" from the processor adds an offset to the PT signal to reduce it by about 50 units. The signal "PLUS100" Which offsets the PT signal by +100 to +130 ADU, is available to allow the processor to measure exactly the value of the "DASH50" offset during auto zero time. During operation, if the A/D reading is 255, the DASH50 signal is asserted, the A/D is read again, and the exact value of the DASH50 offset is added to the A/D reading. The stored zero offset may then be subtracted to obtain the pressure reading.

4.4.2.4 OSCILLATION CHANNEL AMPLIFIER CIRCUIT. U15 provides a low pass filter, a switchable gain amplifier, and two clampable stages of high pass filter. CR6, CR7, and two sections of U15 provide a 0 to 5.0 volt clamp similar to the one in the PT channel.

Means are also provided to characterize the gain and frequency response of the FPT section during calibration mode or wait times. The FPTTEST-1 signal is coupled through a section of buffer U17 into the PT channel ahead of the FPT pickoff point. The gain from this point is such that a controlled amplitude step voltage of about 1 mmHg is passed through the FPT channel. The resulting response can be digitized by the A/D converter and features of the response compared against known correct values, establishing greater confidence in the operation of the analog section.

4.4.2
Analog Subsystem
Continued

4.4.2.5 REFERENCE VOLTAGE SUPPLY CIRCUIT. U19, a programmable shunt regulator, provides an independent 4.50 volt source to set the scale factor of the A/D converter and the excitation current for the pressure transducer, as well as a stable source for the zero reference for the preamplifier and the calibrated 50 mmHg offset. R48 is used to set this voltage to the correct value.

4.4.2.6 POWER SUPPLY VOLTAGE MONITORS. The system supply voltages of +5 volts, +8 volts, -6 volts, plus the battery and line power supplies are connected, through appropriate dividers, to inputs on the A/D multiplexer. These readings are compared against the correct ranges of values to operate the power supply alarms. Additionally, Vbc, the battery charger controller voltage, is used to indicate when line power is available.This information is used, along with the battery voltage, to control the state of the "BATTERY" led.

4.4.3
Switchpanel Interface

The switch panel interface is shown on sheet 3 of the schematic. All the switches on the front panel, except the ON and OFF switches, are wired in a matrix (as shown in Figure 4-7) which is interrogated at a 40 Hz rate by the CPU through the A-to-D converter, U7. An interrogation sequence involves strobing each KEYROW line followed by reading each KEYCOL line to determine which, if any, keyswitch has been pressed. The KEYROW signals, KEYROW0, KEYROW1 and KEYROW2 are developed by the digital I/O bits, DIO0, DIO1 and DIO2, respectively. These digital I/O bits are programmed by the CPU at power-up to be digital output bits and are applied to the switch panel matrix at J2-4, J2-5 and J2-6, through diodes CR15, CR14 and CR13. These diodes prevent +5 Vdc from being applied to the digital outputs should two front panel switches be pressed at the same time. While a digital "one" is applied to one of the KEYROW lines, the KEYCOL lines are read sequentially to determine which keyswitch is pressed. KEYCOL0, KEYCOL1, KEYCOL2 and KEYCOL3 are brought into the CPU board at J2-1, J2-2, J2-3 and J2-4, respectively and applied to analog input channels P0, P1, P2 and P3. These channels are programmed to be digital input channels at power-up. Note that KEYCOL2 is also sent to the pneumatic system reset circuit, shown on sheet 2 of the schematic, to allow the CANCEL switch to reset the overpressure latch on the pneumatic board.

The front panel ON and OFF switches are brought into the CPU board at J2-8 and J2-9, respectively, and sent directly to the power supply through J5-17 and J5-19 as shown on sheet 1 of the schematic.

4.4.4 Display Board Interface

The display board is an output device which is controlled by data transfers from the CPU. Most of the interface circuits are shown on sheet 2 of the schematic. The display board is selected by DSPSEL-0 which is generated by the high order address decode circuit in the gate array, U2. Any I/O data transfer in the range of 0800H to 08FFH will cause U2-39 to be asserted and sent to the display board via E1-9. The low order address bits A0 through A3 are driven directly by the CPU and sent to the display board via E1-11 through E1-14, respectively. The data bits, D0 through D7, are driven directly by the CPU and sent to the display board via E1-18 through E1-25, respectively. Data transfers are synchronized with the CPU by the Q clock, QCLK, which is generated by the gate array at U2-5 and sent to the display board via E1-8.

Supply voltage is brought in from the power supply and routed directly to the display board as shown on sheet 1 of the schematic.

The MAINSLED signal is derived from the battery charger voltage, Vbc, as shown on sheet 3 of the schematic. Vbc is brought in from the power supply at J5-14 and is present only when the AC line power is connected and turned on at the power entry module. This voltage is reduced by R68 and sent to the display board via E1-7 where it is used as drive voltage for the MAINSLED.

4.4.5 Pneumatics Module Interface

The pneumatic module interface is effected at J3 of the CPU board. These signals are shown on all three sheets of the schematic.

The pneumatic valve control signals are ZERO-1, DUMP-0 and DEFLATE-0. The auto zero valve is controlled by ZERO-1 which is a discrete digital output bit generated by the digital latch, U8-16, as shown on sheet 3. When ZERO-1 is true, the auto zero valve applies the pneumatic line from the pressure transducer to atmosphere. When ZERO-1 is not asserted, the auto zero valve applies cuff pressure to the pressure transducer. The dump valve is controlled by DUMP-0 which is a discrete digital output bit generated by the digital latch, U8-19, as shown on sheet 3. When DUMP-0 is true, the dump valve ports the cuff pressure line to atmosphere. When DUMP-0 is not asserted, the dump valve ports the output of the air pump to the cuff pressure line. The deflate valve is controlled by DEFLATE-0 which is a discrete digital output bit generated by the gate array, U2-28, as shown on sheet 2. When DEFLATE-0 is true the deflate valve is de-energized and applies the cuff pressure line to atmosphere. When DEFLATE-0 is not asserted, the deflate valve is energized to block the cuff pressure deflate line.

4.4.5 Pneumatics Module Interface Continued

The air pump control signal (PUMPON-1) is a discrete digital output bit generated by the gate array, U2-31, as shown on sheet 2. When PUMPON-1 is asserted, it enables regulated DC power to be applied to the air pump.

The pneumatic system reset signal, PNEURESET-1, is generated by Q6, Q7, CR1 and CR2 as shown on sheet 2. This signal is used to reset the overpressure signal latch in the pneumatics board and is required to be a positive-going edge whenever the monitor is first turned on or whenever the front panel CANCEL switch is pressed. When the monitor is first turned on, the power supply asserts RESET-0 and holds it low for approximately 50 milliseconds. When RESET-0 is asserted, it forward biases CR1 to hold PNEURESET-1 low and forward biases CR2 to turn off Q6. When RESET-0 goes high, CR1 and CR2 are reverse biased, PNEURESET-1 is asserted by +5 through R83, and C13 begins to charge through R84 and R85. When C13 is charged, Q6 is turned on and PNEURESET-1 is un-asserted. To allow for resetting the overpressure latch by pressing the CANCEL switch, KEYCOL2 is used to gate Q7 which turns off Q6, thus asserting PNEURESET-1 for the duration of the switch panel interrogation pulse.

4.4.6 Fail-safe Timer Circuit

The fail-safe timer circuit is shown on sheet 2 of the schematic. This circuit consists of a crystal-controlled oscillator, a clock divider and a binary counter. It performs two functions: it acts as a fail-safe timer which times out in 4 seconds if not reset by the microprocessor through the gate array, and it provides a crystal-controlled time base for periodic comparison to the microprocessor clock as a system check. U12 is a 7-stage ripple counter which divides the oscillator frequency of 32.768 kHz down to a 2 Hz signal (U12-3) which is used to clock the binary counter, U11.

U11 is reset at power on time by RESET-0 which is generated by the power supply and resets U11 through U10. Thereafter, the microprocessor must periodically generate ZDMANB-0 through the gate array (U2-34) before the binary counter tallies 4 seconds. ZDMANB-0 is capacitively coupled to U10 by C9 to prevent a stuck bit from holding the counter reset. If the microprocessor should fail to generate the reset in some way, U11-6 will go high after 4 seconds since the last reset and hold the clock divider in a clear state at U12-12. When U11-6 goes high it generates the fail-safe alarm, FSALARM-0 through U9-8, which is sent to the pneumatics module through J3-17 where it is used to generate the audio alarm and inhibit the valve drive circuits. The fail-safe alarm at U9-8 is also used to disable the TXEN-0 signal at U10-6 which is sent to the external communication port on the pneumatics module.

4.4.6 Fail-safe Timer Circuit Continued

The third stage of the binary counter (U11-9) is periodically (at least twice a minute) read by the microprocessor as a digital input through the gate array (U2-35) to check the oscillator circuits. If the comparison shows that one of the oscillators is off frequency by more than ±0.5%, the microprocessor generates the 901 alarm and stops monitor operation.

4.4.7 External Communications and Control

The external communications and control circuits are shown on sheet 3 of the schematic. AUXIN-0, AUXOUT-0, RXR-1 and TXE-1 are not supported by the software at this time. The software does support serial communications between the Asynchronous Communications Interface Adaptor (U6) and an external device capable of receiving logic level (0V = MARK, +5V = SPACE) serial communication signals in ASCII format at 600 baud. The received signal, RxD-0, is terminated by a 10k ohm resistor, R72, and applied to the input of a CMOS inverter, U13. CR11 is a 5.1V Zener which allows RS232 logic levels to be applied as signal inputs. The transmit line, TxD-0, is output by the CMOS inverter, U13-4. Refer to Section 3 of this manual for the serial communication protocol.

4.5 PNEUMATIC CONTROL CIRCUITS

The pneumatic control circuits are shown on schematic SC315-292. Functionally, these circuits consist of the valve drive circuits, the pump drive circuits and the overpressure and safety interlocks.

4.5.1 Valve Drive Circuit

The valve solenoids are powered by the +8V supply and energized by digital control of the VMOS FET switches, Q1, Q3 and Q4.

The AUTO ZERO valve, MT1, is energized when Q3 is turned on by ZERO-1. When energized, the AUTO ZERO valve blocks the CUFF input port and connects the pressure transducer to atmosphere. When de-energized, the AUTO ZERO valve connects the pressure transducer to the CUFF input port.

The DUMP valve, MT3, is energized when Q4 is turned on by U2-10. U2-10 goes high when DUMP-0 is asserted or (U3-3) when the fail-safe alarm (FSALARM-0) or the overpressure signal (OP-1) is asserted. When energized, the DUMP valve blocks the output of the air pump and ports the CUFF pressure port to atmosphere. When de-energized, the DUMP valve ports the output of the air pump to the CUFF pressure port.

4.5.1
Valve Drive Circuit
Continued

The DEFLATE valve, MT2, is energized when Q1 is turned on by U2-4. This occurs when either the DEFLATE-0 is unasserted, or FSALARM-0 or OP-1 is asserted. When the DEFLATE valve is energized, the deflate line from the CUFF pressure port is blocked. When the DEFLATE valve is de-energized, the deflate line is ported to atmosphere through a restrictor in the DEFLATE valve common port tubing. Zener diode, D1, provides for a faster collapse of the solenoid fields of MT2 and MT3.

Resistors R25, R26 and R27 provide an average voltage reading, VLVSENSE, indicative of the current drain of all three solenoids which is used in manufacturing tests.

4.5.2
Pump Drive Circuit

The unregulated pump voltage, Vp, from the power supply is applied to the pump through Q2 and is regulated by U1. U1 is a pulse width modulator whose open-collector outputs drive the base of Q2. The R-C circuitry causes the modulator to operate at about 5 kHz. The outputs of the modulator are turned on and off by the shutdown, SD, input which is driven by U2-11. When PUMPON-1 is asserted, and providing the DEFLATE valve is energized (closed), the modulator is turned on to provide a regulated 12 Vdc to the pump motor through Q2.

4.5.3
Overpressure Switch and Safety Interlocks

The overpressure switch is fed by a pneumatic line from the CUFF pressure port with a restrictor inline. The restrictor prevents pressure transients from falsely triggering the overpressure switch. The switch is set to trigger in the range of 265 mmHg to 355 mmHg. The normally-closed contacts of the overpressure switch pull U3-12 to ground to hold the NOR latch in the reset state. When an overpressure condition trips the switch, the contacts open and the NOR latch is set by +5 V through R6 to assert OP-1. OP-1 enables U3-3 to energize the DUMP valve and de-energize the DEFLATE valve to dump cuff pressure and turn off the pump (U2-12). OP-1 also turns on Q7 which provides a back-up to energize the DUMP valve in the event Q4 fails. The CPU reads the OP-1 signal as a digital input bit to generate the 800 visual and audible alarm. When the overpressure switch closes, the NOR latch may be reset by PNEURESET-1 at U3-8. Capacitor, C1, prevents a stuck PNEURESET-1 from holding the latch in the reset state. PNEURESET-1 is generated on the CPU board by the trailing edge of RESET-0 or by the leading edge of KEYCOL2 (CANCEL switch depression).

The fail-safe alarm interlocks are effected by U3-3 which disables U2 when the fail-safe alarm occurs (FSALARM-0). Thus, a fail-safe alarm will cause the DUMP valve to energize, the DEFLATE valve to de-energize and the pump drive circuit to be disabled. The output at U3-4 will also cause the audio annunciator circuit to generate the highest volume, constant audio alarm.

4.6 AUDIO ANNUNCIATOR SYSTEM

The audio annunciator system (shown on schematic SC 315-292) consists of switching transistor (Q5), volume control transistor (Q6), voltage converter (U4), and the Piezo annunciator module (AL1). During normal operation, the audio alarm is controlled by BEEPER-1 which is generated by the CPU. BEEPER-1 is a pulse-modulated digital signal which drives the base of Q5. The R-C network in the collector circuit of Q5 applies base drive to Q6 which is proportional to the duty cycle of BEEPER-1. The voltage converter, U4, applies a voltage differential across AL1 in the range of 0V to about 15V proportional to the resistance of the emitter -collector junction of Q6. The Piezo alarm module, AL1, is an integral oscillator and annunciator which operates at a fixed frequency of 3000 Hz. The alarm may be disabled by connecting J1-15 to J1-1 or J1-7 on the external communication connector to assert ALMDIS-0.

4.7 DISPLAY BOARD

The display board circuits are shown on schematic, SC 315-288, contained in Section 6. The functional circuits that comprise the display board are:

- the Seven-segment displays,
- the Discrete LED's,
- the Display Data Transfer Timing Circuits,
- the Scan Failure Protection and Ghosting Prevention Circuits, and
- the Temperature Conversion Circuit.

4.7.1 Seven-Segment Displays

The seven-segment displays are shown on sheet 2 of the schematic. These are grouped and identified as CYCLE, TEMPERATURE, SYSTOLIC, PULSE and DIASTOLIC. Each digit display is a common-cathode array of seven segments and a decimal point. The seven segments, plus decimal point, are driven by the 2907 PNP transistors, powered by the +5 supply, as shown on sheet 1 of the schematic. Base drive for these transistors is provided by the LM324 linear op-amps which are switched by the output of the data latch, U1, shown on sheet 1. The common cathode connections for each digit display are individually pulled to ground by the outputs of the address latch, U7-U8, through the NPN Darlington drivers, U5-U6.

4.7.2 Discrete (point) LED Displays

The discrete (point) LED's are shown on sheets 1 & 2 of the schematic. Those shown on sheet 2 have their cathodes pulled to ground by U6-11 when the address latch bit DG14 is asserted. Each LED of this group is driven by the +5 V supply through the 2907 PNP transistor (shown on sheet 1) selected by the state of the data latch, U1. The discrete LED's shown on sheet 1 have their cathodes pulled to ground by the common collector outputs of the data latch, U14. The data latch is selected by the leading edge of the address decode, DG15, generated by U8 as shown on sheet 2.

4.7.3 Display Data Transfer Timing

The display data transfers between the CPU and the display board are controlled by various NAND gates in U12, the data latch (U1), and the address latch (U4) as shown on sheets 1. When output data (D0-D7) is written by the CPU to any address in the range of 0800H through 0FFFH, the signal DSPLSEL-0 is asserted by the gate array on the CPU board. DSPLSEL-0 causes U12-3 to enable the latch trigger circuit at U12-5 so that the trailing edge of QCLK will latch the data (D0-D7) at U1-11 and the address (A0-A3) at U4-9.

The data latch, U1, is a CMOS octal D-type flip-flop whose Q outputs (LD0-LD7) are applied to the inverting inputs of linear op-amps U9-U10, as shown on sheet 2. When the output of any op-amp goes true (high), the associated driver transistor is turned on to apply +5V segment drive (or point LED drive) to the address-selected display.

The address latch, U4, is a CMOS quad D-type flip-flop whose outputs are used to steer and gate the inputs of the octal address decoders, U7 and U8. The decoded address (DG0 - DG15) is used to select the digit (or point LED group) by pulling the cathode to ground through its associated NPN Darlington driver (U5 - U6). The decoding of the latched address is delayed by approximately 10 microseconds after the leading edge of DSPLSEL-0 to prevent ghosting due to propagation delays. The decoding lasts until the leading edge of the next DSPLSEL-0 which occurs in response to the FIRQ (1200 Hz) interrupt to the CPU.

4.7.4 Scan Failure Protection and Ghosting Prevention

Scan failure protection and ghosting prevention is provided by a dual CMOS multivibrator, U13. One half of U13 is configured to be a retriggerable one-shot at U13-6 with a period of 2 - 20 milliseconds (scan failure protection), and the other half is configured to be a 10 microsecond one-shot at U13-9 (ghosting prevention).

The output at U13-6 remains high as long as DSPLSEL-0 is asserted in response to the FIRQ interrupt. Should the microprocessor fail to address the display in response to the FIRQ interrupt or the gate array fail to generate the DSPLSEL-0 signal, U13-6 will go low when the one-shot times out (2 - 20 milliseconds) and disable the address decode circuits to prevent the last selected LED from being overdriven.

The output at U13-9 goes low for 10 microseconds after DSPLSEL-0 (DSPLSEL-0 is approximately 1 microsecond in length) to delay the decoding of the address by U12-11 and, thus, prevent ghosting due to propagation delays.

4.7.5 Temperature Conversion Circuit

The temperature conversion circuits provide for temperature detection, digital conversion , auto-calibration and patient isolation. The temperature probe contains a thermistor which exhibits a precisely calibrated negative temperature coefficient of resistance. The thermistor is connected into a network comprising a precision resistance and voltage reference. The output of the network is a voltage that varies proportionally with temperature and linearily in the temperature range about normal body temperature. Nonlinearities outside this range are corrected in software.

The voltage from the thermistor input network is digitized using a voltage-to-frequency converter (VFC). The 8100T software system measures the output frequency by counting transitions during a controlled gate interval which is proportional to the voltage output from the thermistor network. The specified accuracy of the Model 8100T requires greater stability in the A/D conversion than is provided by the long-term stability of the VFC. To meet the specification, a method of automatic calibration under software control is employed.

The input to the VFC is selected from among four sources by an analog multiplexer, one input of which is the thermistor network. The other three inputs are reference voltages derived from the same excitation voltage source as the thermistor network.

The software can measure the known references and adjust the scale and offset of the measurements to cause the conversions to be correct. Thus, the system accuracy depends only on the stability and accuracy of the reference divider and thermistor input resistors. Variations in scale factor and offset due to temperature coefficients or long term drifts of the reference voltage or the VFC and associated circuitry can be cancelled. This system also provides a self test capability and a means of detecting temperature probe type (oral or rectal).

The temperature conversion circuits are shown on sheet 3 of schematic SC315-288 and comprise

- the isolated power supply,
- the precision reference voltage supply,
- the temperature probe thermistor interface,
- the temperature calibration and probe type detector,
- the temperature channel selector,
- the voltage-to-frequency converter, and
- the data isolators

4.7.5 Temperature Conversion Circuit Continued

4.7.5.1 Isolated Power Supply. Isolation for the temperature converter power is provided by an inverter which is supplied from the monitor +8Vdc supply at J1-5. Q1 and Q2, with associated components, comprise an astable multivibrator operating at 30 kHz nominal. The collector current flows through the primary of T1, a ferrite pot core transformer. A square wave appears at the secondary of T1 and is full wave rectified and filtered by CR1, CR2, and C7. Nominal output is +9Vdc.

4.7.5.2 Precision Reference Voltage Supply. A precision adjustable shunt voltage regulator, U15, provides the regulated reference voltage source (+3.24 Vdc, nominal) for the thermistor input network, the reference network, and the VFC reference network. The reference is adjustable to compensate for initial tolerances in the VFC (U16) and timing capacitor (C6), thereby, centering the dynamic range of the automatic calibration algorithm.

4.7.5.3 Temperature Probe Thermistor Interface. The excitation voltage and the load resistance are provided by R40 and R41. The thermistor is in parallel with R40. As the temperature increases the thermistor resistance decreases, causing the voltage at the junction of R40 and R41 to increase. The values of these resistors were selected to locate a linear temperature-to-voltage function around normal body temperature and to set the excitation voltage for maximum output without excessive self-heating effects at the thermistor.

4.7.5.4 Temperature Calibration and Probe Type Detector. A voltage divider comprising R44 - R47 divides the reference voltage into two voltages representing 10° C and 37° C. R42 and R43 trim the 37° C reference for minimum error at the most tightly specified accuracy point. The software periodically reads the voltages for 10° C (channel 0) and 37° C (channel 1) and adjusts the offset and scale factors for zero error at these two points, thus cancelling the effects of drifts in the VFC and reference voltage. A voltage divider comprising R63 - R66 provide a 42° C reference voltage (channel 2) which is read for self test of the temperature circuit and for identification of the probe type. When the rectal probe is attached, a jumper in the probe connector shorts E4 to E5 (pins 2 & 7) effectively shorting out R63 which shifts the 42° C standard slightly higher and allows the software to identify the probe type. This is necessary for the software to accurately predict a rectal temperature when in **NORMAL** mode.

4.7.5.5 Temperature Channel Selector. A CMOS analog multiplexer, U17, switches the input to the VFC among the three calibration sources or to the probe interface. The input is selected by the software via the two bits from the data latch, U14, which are patient-isolated by optoisolators U19 & U20.

4.7.5
Temperature Conversion Circuit Continued

4.7.5.6 Voltage-to-Frequency Converter. The voltage-to-frequency converter, U16, is a monolithic VFC whose output is a square wave at a frequency determined by C6 and the current drawn from pin 3. The voltage at pin 3 follows the input voltage applied to pin 4 by virtue of an internal op-amp. Pin 3 is connected to the reference voltage through network R48 and R49 which (by Thevenin's Theorem) is equivalent to a voltage source behind the parallel combination of resistances R48 and R49. The current out of pin 3 is, therefore, proportional to the difference between the input voltage at pin 4 and the open circuit voltage that would appear at the junction of R48 and R49 if U16 were disconnected. The combination results in a VFC with a scale factor and input offset established by the reference voltage , C6, R48, and R49.

4.7.5.7 Data Isolators. The square wave output of U16 is transmitted to the CPU board at JMP22 (digital input port) by optoisolator U18. The control bits (SEL0, SEL1) from the data latch, U14, are isolated by optoisolators U19 & U20.